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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
Edwin C. Kan et al.) Group Art Unit No. 2818
Application No. : 10/718,662) Examiner:
Filed : November 24, 2003)
For : Multibit Metal)
Nanocrystal Memories)
and Fabrication)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions of 37 CFR 1.97 and 1.98, applicants hereby submit the documents listed on the attached PTO-1449B.

Copies of the cited publications are enclosed. Copies of the cited patents have not been included, but will be furnished upon request.

Respectfully submitted,

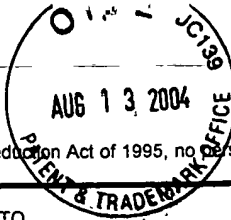
Edwin C. Kan et al.
Applicant

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Attorneys for Applicant

By: 

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August 13, 2004



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| Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) | | | | Complete if Known | |
| | | | | Application Number | 10/718,662 |
| | | | | Filing Date | November 24, 2003 |
| | | | | First Named Inventor | Edwin C. Kan |
| | | | | Art Unit | 2818 |
| | | | | Examiner Name | |
| Sheet | 1 | of | 3 | Attorney Docket Number | CRF D-2768D/Kan |

| NON PATENT LITERATURE DOCUMENTS | | | |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | 1 | "The Evolution of Dram Cell Technology," B. El-Kareh, G.B. Bronner; Solid State Technology, May 1997, Vol. 40, Issue 5 | |
| | 2 | "Fast and Long Retention-Time Nano-Crystal Memory," H.I. Hanafi, S. Tiwari, I. Khan; IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996 | |
| | 3 | "Charge-Trap Memory Device Fabricated by Oxidation of Si _{1-x} Ge _x ," Y-C King, T-J King, C. Hu; IEEE Transactions on Electron Devices, Vol. 48, No. 4, April 2001 | |
| | 4 | "A Long-Refresh Dynamic/Quasi-Nonvolatile Memory Device with 2-nm Tunneling Oxide," Y-C King, T-J King, C. Hu; IEEE Electron Device Letters, Vol. 20, No. 8, August 1999 | |
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| | 7 | "High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application," H.C. Wann, C. Hu; IEEE Electron Device Letters, Vol. 16, No. 11, November 1995 | |
| | 8 | "Programming Characteristics of P-Channel Si Nano-Crystal Memory," K. Han, I. Kim, H. Shin; IEEE Electron Device Letters, Vol. 21, No. 6, June 2000 | |
| | 9 | "A Novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications," J. DeBlauwe, M. Ostraat, M.L. Green, G. Weber, T. Sorsch, A Kerber, F. Klemens, et al.; 2000 IEEE | |

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| | 10 | "Single-Electron Devices and Their Applications," K.K. Likharev; Proceedings of the IEEE, Vol. 87, No. 4, April 1999 | |
| | 11 | "Non-Volatile Si Quantum Memory with Self-Aligned Doubly-Stacked Dots," R. Ohba, N. Sugiyama, K. Uchida, J. Koga, A. Toriumi; IEEE 2000 | |
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| | 13 | "Room Temperature Operation of a Quantum-Dot Flash Memory," J.J. Welser, S. Tiwari, S. Rishton, K.Y. Lee, Y. Lee; IEEE Electron Device Letters, Vol. 18, No. 6, June 1997 | |
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| | 16 | "Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan; 1995 IEEE | |
| | 17 | "Multilevel Flash cells and their Trade-offs," B. Eitan, R. Kazerounian, A. Roy; G. Crisenza, P. Cappelletti, A. Modelli; 1996 IEEE | |
| | 18 | "Modeling and Design Study of Nanocrystal Memory Devices," M. She, Y-C King, T-J King, C. Hu; Dept. of Elect. Eng. and Comp. Sciences, U. of C., Berkely, CA | |
| | 19 | "A Four-State EEPROM Using Floating-Gate Memory Cells," C. Bleiker, H. Melchior; IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987 | |

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| | 20 | "A Multilevel Approach Toward Quadrupling the Density of Flash Memory," D.L. Kencke, R. Richart, S. Garg, S.K. Banerjee; IEEE Electron Device Letters, Vol. 19, No. 3, March 1998 | |
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